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To date, a rising need for high-speed low-noise electronic devices is observed for a wide variety of applications, including wireless or fiber communications. Low-frequency noise poses a lower limit on the signal level in broadband circuits. Noise sources are related to various kinds of materials imperfections such as point or line defects, but also to interface interface defects or defects at contacts. As device dimensions decrease, the noise introduced by trapping-detrapping of carriers at deep defects becomes increasingly important. Therefore, the analysis of low-frequency electrical noise can be a useful tool not only for the qualification of device performance, but also for the characterization of noise-generating deep level defects in semiconductor materials. The advantages of this technique include the possibility of measuring fully processed device structures and the direct relevance of the measured defect characteristics to device performance Reduction of the noise level frequently requires the correct identification of noise sources. However, difficulties can arise in the interpretation of often-indistinct noise spectrum features.

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## Table of Contents

## Abstract

To date, a rising need for high-speed low-noise electronic devices is observed for a wide variety of applications, including wireless or fiber communications. Low-frequency noise poses a lower limit on the signal level in broadband circuits. Noise sources are related to various kinds of materials imperfections such as point or line defects, but also to interface defects or defects at contacts. As device dimensions decrease, the noise introduced by trapping-detrapping of carriers at deep defects becomes increasingly important. Therefore, the analysis of low-frequency electrical noise can be a useful tool not only for the qualification of device performance, but also for the characterization of noise-generating deep level defects in semiconductor materials. The advantages of this technique include the possibility of measuring fully processed device structures and the direct relevance of the measured defect characteristics to device performance Reduction of the noise level frequently requires the correct identification of noise sources. However, difficulties can arise in the interpretation of often-indistinct noise spectrum features. The DURIP grant allowed to acquire a state-of-the-art low-frequency noise analysis system with variable-T probe station that has been set up for use by all interested faculty and their students at UC Berkeley. This report presents some typical examples for the current usage of the system and points out areas of future usage.

# 1. Introduction

The field of noise measurements is quite mature and is the subject of a large amount of literature. Most of these works focus on either device noise performance from the engineering end, or noise sources and models from the physics and mathematical end. A comparatively small amount of literature has dealt with the measurement of point defects and their properties from low frequency noise measurements (LFNM). As device sizes are reduced, however, the noise due to traps takes on increased importance. At the same time measurements of traps in these ultra-small structures by standard techniques like deep level transient spectroscopy (DLTS) and its variants becomes more difficult. In view of these trends, the use of LFNM for defect measurements is reviewed. The application of LFNM to a particular structure (GaAs-on-insulator (GOI) MESFETs) for which DLTS is difficult is demonstrated (chapt. 4). Also, examples for measuring noise in silicon-based devices are given (chapt. 5).

The low frequency noise present in common semiconductor devices can be divided into three types: white, 1/f, and generation-recombination (g-r) noise. These noise types will be briefly introduced to explain their role in LFNM. For details regarding derivations and more complex systems, noise texts, e.g. [1,2], should be consulted.

White noise has a uniform distribution of noise power across the frequency band of interest. By integrating the noise power spectrum, it is clear that white noise cannot extend with constant power to infinite frequency, but must instead have a roll-off beginning at some corner frequency. For shot noise and thermal noise, the two primary sources of white noise, this corner frequency lies in the gigahertz range, well above the standard 0.1-1 MHz upper bound to low frequency noise measurements. It must be noted that shallow traps can cause generation-recombination noise (discussed below) with a corner frequency above 1 MHz, giving the appearance of white noise in the low frequency range. High-quality precision resistors serve as excellent sources of white noise that can be used to calibrate noise measurement systems. The relevant current noise power $S_I$ generated is related to resistance R, the temperature T, and current I:

$$\text{thermal noise: } S_I = 4kTR \qquad (1.1)$$

$$\text{shot noise: } S_I = 2qI \qquad (1.2)$$

where k is Boltzmann's constant. The temperature- and current-dependence of the observed noise allows a simple determination of the dominant noise source.

Flicker noise, or 1/f noise, is often a major component of low frequency noise and may obscure the generation-recombination noise spectrum of interest. As the name implies the 1/f noise power is inversely proportional to the frequency. There are numerous proposed sources of 1/f noise [3], but the structure-less nature of the spectrum often makes it difficult to identify the mechanism responsible. In devices, likely sources of 1/f noise are surfaces and interfaces where a band of states may exist. The overlapping generation-recombination spectra from these states, which have a wide range of different time constants, appear like a featureless 1/f spectrum. Therefore, devices with well-controlled surfaces bounding the current path (e.g. gated devices) have the best chance for showing noise due to bulk traps.

Generation-recombination noise is the noise type that will be emphasized here as it is of the most interest to materials science. It is important to note that the term generation-recombination does not imply the usual sense of band-to-band processes. Instead, the recombination process indicated is the capture of a carrier from a band and conversely generation is the emission of a carrier from a trap back into that band. For simplicity, only mono-polar devices will be considered. When both electrons and holes play a significant role in the device operation, noise analysis is greatly complicated because processes like electron-hole recombination through trap levels must be analyzed, and the electron and hole concentrations in bipolar devices often vary by orders of magnitude over small dimensions. In the mono-polar case and neglecting any fluctuation in the mobility, a resistor has a fluctuating resistance depending only on the fluctuation in the carrier concentration. Considering a single set of traps, in an n-type semiconductor, the carrier concentration fluctuation depends on the exchange of electrons between the conduction band and the trap level. The differential equation describing the concentration of electrons in the conduction band n comprises a term representing the capture of electrons into traps and a term representing their re-emission:

$$\frac{dn}{dt} = -v_{th}\sigma(N_T - n_T)n + Ae^{-E_A/kT}n_T \qquad (1.3)$$

where $v_{th}$ is the thermal velocity, $\sigma$ is the capture cross section, $N_T$ is the total trap density, $n_T$ is the filled trap density, A is a prefactor term representing an escape attempt rate ($s^{-1}$) and $E_A$ is the activation energy for removing the electron from the trap. In equilibrium, dn/dt=0. This equality only applies over a time average; electrons are continually exchanged between the conduction band and the trap states. The capture and emission processes establish two time scales - a capture time constant $\tau_c$ and an emission time constant $\tau_e$:

$$1/\tau_c = v_{th}\sigma(N_T - n_T) \qquad (1.4)$$

$$1/\tau_e = Ae^{-E_A/kT} \qquad (1.5)$$

To solve Equation (1) a single time constant is introduced: $1/\tau=1/\tau_c + 1/\tau_e$. The solution for the carrier concentration as function of time is a simple exponential. To obtain the power spectrum the Fourier transform is taken. The determination of the magnitude of the spectrum accounts for the noise contribution of each individual trap. The derivation is somewhat complex requiring the evaluation of the expectation value of the standard deviation of the filled trap density. In the interest of space the result for the current noise power spectral density $S_I$ will be taken from [4]:

$$\frac{S_I}{I^2} = \frac{2\tau}{n^2V}\frac{n_T(N_T - n_T)}{N_T}\frac{1}{1+(2\pi f\tau)^2} \qquad (1.6)$$

where V is the volume of the device. Two important things can be seen from this equation. First, the smaller the device volume, the larger the g-r noise power for a given current I. Therefore reduced device sizes give more sensitive g-r noise measurements. Second, the noise is a maximum when the traps are half full; when the trap energy is far from the Fermi level the g-r noise is reduced.

In devices such as MESFETs the channel is relatively highly doped so that the Fermi level is near the conduction band. Then almost all traps are filled ($N_T$~$n_T$), and the capture time constant $\tau_c$ is very long. Therefore the emission time constant $\tau_e$ determines $\tau$ and a standard Arrhenius plot allows the determination of $E_A$ in analogy to DLTS. Similarly, the y-intercept of the Arrhenius plot allows the determination of the capture cross section because the constant A in (1.3) is related to $\sigma$ through the principle of detailed balance.

## References, chapt. 1

[1] A. van der Ziel, *Noise in Solid State Devices and Circuits, Wiley, 1986.*
[2] A. Ambrozy, *Electronic Noise, McGraw-Hill, 1982*
[3] e.g., the papers in the series *Quantum 1/f Noise and Other Fluctuations in Electronic Devices*, P.H. Handel and A.L Chung, eds., *AIP Press*
[4] J.A. Copeland, "Semiconductor Impurity Analysis from Low-Frequency Noise Spectra", *IEEE Trans. Electron Devices* ***ED-18****, 50 (1971)*

## 2. Experimental Setup

The basic experimental apparatus for measuring low frequency noise is relatively simple. The device to be measured is mounted in an electro-magnetically shielded environment, such as a metal-enclosed probe station with a single, low resistance ground path. The sample temperature is maintained using a thermoelectric chuck. Care must be taken to allow the temperature to stabilize before measurement because relative motion of the probes and the sample during measurement due to different thermal expansions as the temperature changes can result in spurious noise signals.

Figure 2.1 shows the low frequency measurement setup. The configuration is as supplied by Celestry Design Technologies. The system uses an HP4145 Semiconductor Parameter Analyzer to supply a constant bias voltage (or bias current). Noise is removed from the input using simple RC filters. In most cases it is sufficient to use RC = 0.1 s, though the R value can be selected to deliver filter time constants 1 s of or 0.01 s instead. Following the filter resistor is another selectable resistor, Rd. This is the load resistor that is used to generate the noise signal. The value of the load resistor is selected based on the measured device conductance. For the noise signal to be measured (e.g., the drain current noise of a MESFET), the load resistor is placed between the device terminal of interest and the bias supply. The device under test (DUT) is mounted in a dark box so that a positive bias at D/C forward biases the device. The n-side of the device is grounded.

The noise signal is picked up at the D/C terminal and the ac component is delivered to either a voltage preamplifier or a current preamplifier through a dc blocking capacitor. Typically, the voltage amplifier was used because of the low device output resistance. The amplifiers are powered by large rechargeable lead-acid batteries to minimize the excess input noise. The preamplifier output is fed into a voltage amplifier with a gain of 25, giving a total amplification factor of 500x. The final output signal is fed to a HP 67730 Dynamic Signal Analyzer. All equipment and communication is controlled by computer and allows the direct calculation of the DUT noise power, including correction

for the thermal shot noise contributed by the load and filter resistors. The typical noise floor is ~$10^{-24}$ $A^2$/Hz through the whole range from 1 Hz to 102.4 kHz.

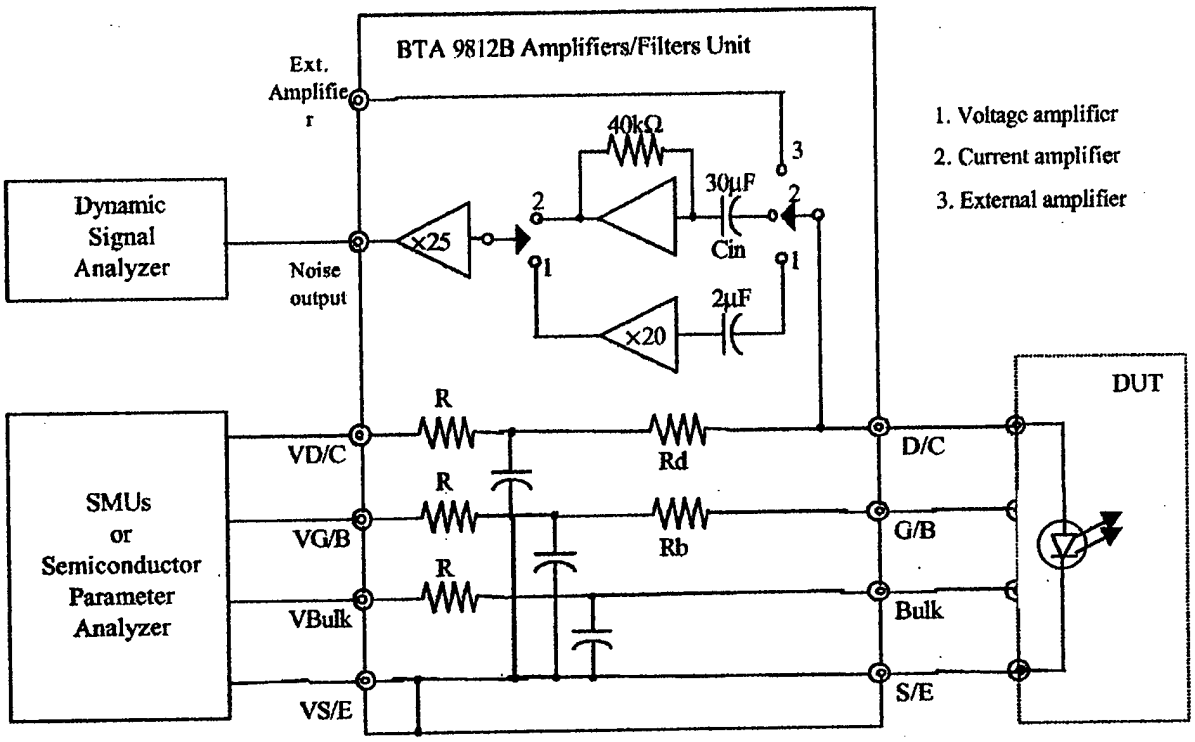


***Figure 2.1. Low frequency noise measurement apparatus. The n-side of the device under test (DUT) is connected to the S/E connection, and the p-side is connected to the D/C connection. (Positive bias is applied to the D/C connection to forward bias the device).***

The low frequency measurement apparatus and probe station described here were installed in the summer of 2001. A first test measurement on highly radiation-damaged silicon was soon successful in demonstrating the application of the technique to defect-dominated materials as shown below. Since then the apparatus has been primarily devoted to measurements of irradiated MESFETs on oxidized AlAs, the so-called GaAs-on-insulator (GOI) technology (chapt. 4), first measurements on III-nitride based structures (chapt. 4.3) and Si-based devices (chapt. 5). A preliminary measurement on an LT-GaAs resistor and measurements on oxide-confined vertical cavity surface emitting lasers in a collaboration with Agilent Technologies are not included here.

## 3. Calibration of the Noise System

Highly radiation-damaged silicon was used to calibrate the low-frequency noise system for noise spectroscopy. This material is known to contain concentrations of the silicon divacancy on the order of $10^{14}$ $cm^{-3}$, and the concentration of residual shallow donors is known to be on the order of $10^{12}$ $cm^{-3}$. It serves as an excellent example of

determining the defect energy in a material dominated by a single deep level. The silicon divacancy is well known to have an energy level at Ec-0.43 eV.

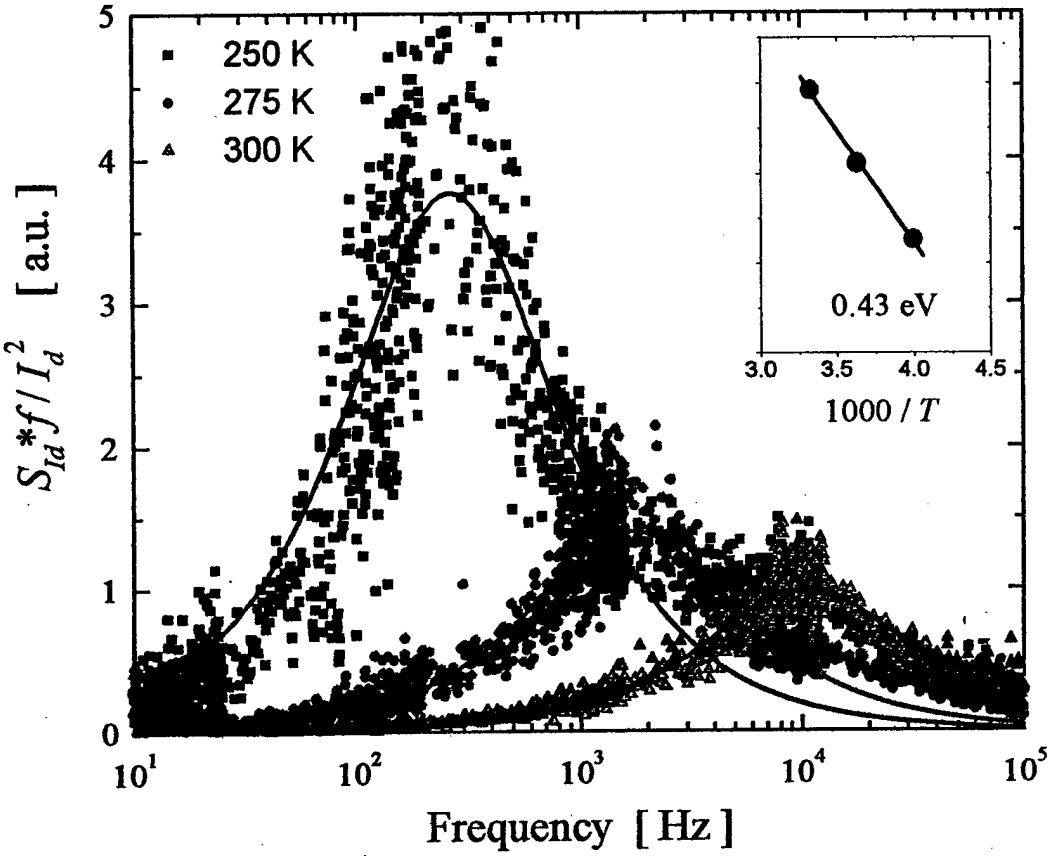


*Figure 3.1: Noise spectra of irradiated silicon diode. The ordinate is the current noise times the frequency, normalized to the dc forward current level. The lines are a Lorentzian fit to the data. Inset: Arrhenius plot of trap emission rate with an activation energy of 0.43 eV*

Figure 3.1 shows a selection of spectra taken on a diode fabricated from the silicon irradiated with 55 MeV protons ($2\times10^{14}$ cm$^{-2}$ dose). To emphasize the presence of a peak in the data, the usual spectrum of current noise per bandwidth (in A$^2$/Hz) is multiplied by the frequency and divided by the dc forward bias current. The peak position clearly shifts to the right at higher measurement temperatures. This results from more rapid carrier de-trapping as the temperature increases. By fitting a Lorentzian spectrum (solid line), a corner frequency can be determined.

The inset shows the variation in the corner frequency with temperature giving an activation energy of 0.43 eV, exactly matching the known value. Measurements at a range of currents have shown that the corner frequency has a very slight shift with increasing current, suggesting it will be possible to extract information regarding hole capture rates and field-enhanced emission. The determination of the total concentration of silicon divacancies is complicated in this sample because the sample structure involves a p-i-n diode instead of a simple resistor. This means that there will be electron concen-

tration gradients through the intrinsic layer. The magnitude of the trap noise depends on the local electron concentration, so the total trap noise is a summation of the total noise emitted at each point in the sample volume. In a uniform resistor, this problem will not be encountered.

# 4. First results – E.R. Weber research group

## 4.1 GaAs-On-Insulator Metal-semiconductor Field Effect Transistors

Lateral selective wet-oxidation of buried high aluminum content $Al_xGa_{1-x}As$ layers has seen widespread application in electrical and optical devices. The oxidized layer is used to provide current confinement and a low refractive index layer in Bragg mirror stacks for vertical-cavity surface emitting lasers, [2, 3] and to serve as a current confining layer in heterojunction bipolar transistors. [4] Another use of this oxidation technique is to form an insulating buffer layer underneath the active channel of metal-semiconductor field effect transistors (MESFETs), [5] so-called GaAs-On-Insulator (GOI) MESFETs. A major concern is that the oxidation procedure can cause defect injection into adjacent layers. In particular, carrying out the oxidation longer than needed to achieve full lateral oxidation of the AlGaAs layer (over-oxidation) is found to have deleterious effects on device performance. [6] Many characterization techniques have been applied to study the oxide microstructure and the GaAs/oxide interface structure, for example transmission electron microscopy (TEM). [7] It has been shown by time-resolved photoluminescence that the interface recombination rate was greatly increased after oxidation. [8] The interface recombination velocity was estimated using the light-beam induced current technique. [9] To date, no direct comparison between the parameters of the oxidation and the formation of specific recombination centers has been reported.

GOI MESFETs were designed and fabricated by applying lateral oxidation to a conventional GaAs FET design. The device structure was grown by MBE on a (100) semi-insulating GaAs substrate and consists of a 75-nm AlAs oxidation layer followed by a 250-nm GaAs channel. The channel was doped with $2\times10^{17}$ $cm^{-3}$ silicon. The structure was capped with a 5-nm $Al_{0.3}Ga_{0.7}As$ gate recess etch-stop layer and a highly doped ($n>10^{18}$ $cm^{-3}$) graded InAs/GaAs digital alloy in order to reduce the contact resistance. No oxidation barrier layers were employed between the oxidation layer and the channel. Devices with gate widths, $w_G$, of 40, 100, and 300 μm were processed on the same wafer. All devices studied here have a gate length of 3.5 microns. After the mesa etch, the AlAs layer was laterally wet oxidized at 430°C in an atmosphere defined by bubbling 500 sccm nitrogen through water at 90°C. The oxidation was carried out for 80 minutes with the goal of just completely oxidizing the widest (300 μm) device. Consequently, the 40 μm gate width devices were heavily over-oxidized.

The total noise-power spectrum can be broken down into the following sum:

$$S_I(f) = C + A/f + \sum_i L_i/\left(1+\left(f/f_{c,i}\right)^2\right). \qquad (4.1)$$

Here, $f_{c,i}$ and $L_i$ are the Lorentzian g-r noise corner frequency and amplitude for the $i^{th}$ trap level. $C$ and $A$ indicate the amplitude of white and 1/f noise components. Since 1/f noise is usually a major component of the observed noise spectrum, the spectral power

density is plotted here as $S_I(f)\times f$ vs. $f$ to reveal g-r noise as peaks. The amplitude $L$ of the Lorentzian component can be expressed as: [10]

$$L \propto I^2 \tau D / n^2 V \tag{4.2}$$

where $D$ is the density of the trap levels, $\tau$, equal to $1/2\pi f_c$, is the characteristic time constant, $n$ is the carrier density, and $V$ is the sampled volume. For traps located more than a few $kT$ ($k$ is Boltzmann's constant) below the Fermi level, the characteristic time constant is determined by the emission rate of the traps.

Several noise power spectra revealing a clear Lorentzian noise component under various experimental conditions are shown in Fig. 4.1. The applied drain voltage was chosen in the ohmic, linear region of the MESFET device characteristics in order to ensure a resistor-like behavior with nearly uniform semiconductor cross-sectional area under the gate. Fig. 4.1(c) shows that at 375K the signal was only observable in the 40 μm and 100 μm gate widths, that is, only when over-oxidation had taken place.

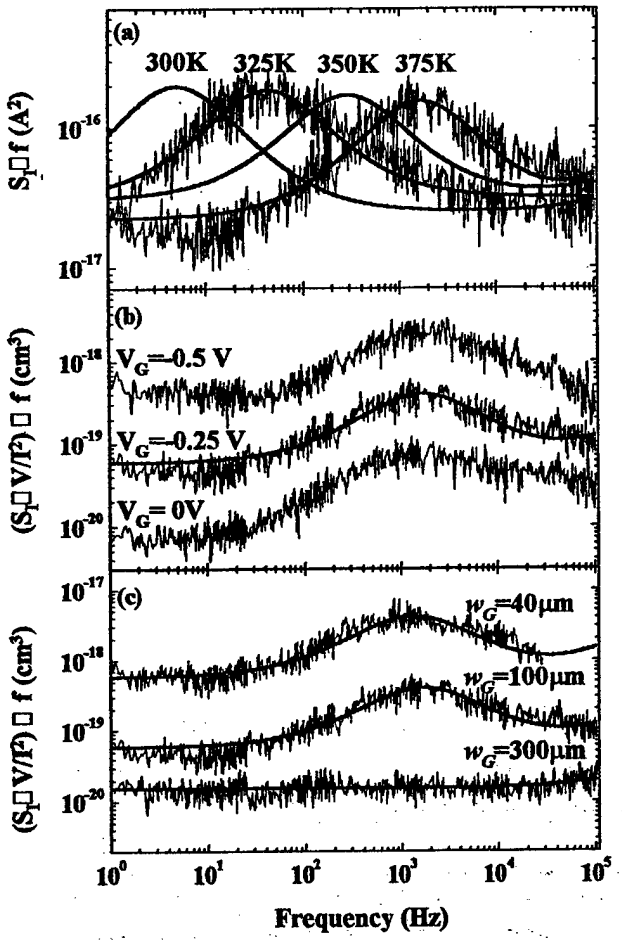


*Figure 4.1: (a) Temperature dependent noise power spectra ($w_G$=100μm, $V_D$=0.2V, $V_G$=-0.25 V); (b) normalized spectra at different gate biases ($w_G$=100μm, $V_D$=0.2V, T=375K); (c) normalized spectra for different gate widths ($V_G$=-0.25V, $V_D$=0.2V, T=375K)*

In-depth analysis of the corresponding trap was achieved by least-squares fits of Eq. (4.1) to the experimental data (solid lines in Fig. 4.1). In Fig. 4.1(a), the corner frequency increases as the thermal emission rate increases with temperature. The time constant $\tau$ times $T^2$ is plotted in Fig. 4.2 to extract the energy level of the trap using the expression $\tau = c\ T^2\ \exp(E_A/kT)$, where $c$ is a constant, and $E_A$ is the activation energy. While the Lorentzian noise signature featured in Fig. 4.1 is due to a g-r level at $E_c$-0.69 eV, additional levels at $E_c$-0.47 and $E_c$-0.32 eV were observed under different gate bias conditions in a typical 100 μm gate-width device, as indicated in Fig. 4.2. The trap energies were found to be independent of the applied drain voltage. The level at $E_c$-0.47 eV appeared only at larger gate biases while the level at $E_c$-0.32 eV appeared at gate biases below the threshold voltage. $E_c$-0.47 eV may be related to a surface conduction processes. [11] The predominating near mid-gap trap at $E_c$-0.69 eV was detected under all gate biases.

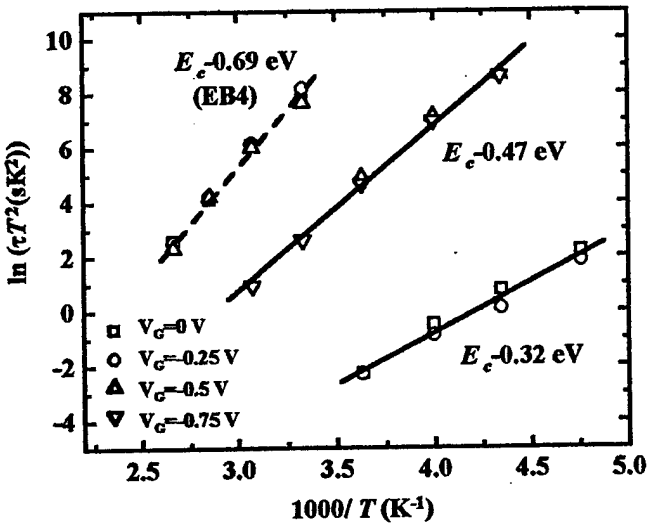


*Figure 4.2: Arrhenius plot of traps in 100μm gate width GOI MESFETs at different gate biases and a drain bias of 0.2 V. Solid lines are the straight-line fits to the experimental data. The dotted line shows the published emission rate of the EB4 trap. [1]*

The depth distribution of the $E_c$-0.69 defect was probed by analyzing the gate-voltage dependence of the Lorentzian-noise signal magnitude, Fig. 4.1(b). A normalization motivated by Eqn. (4.2) was applied in order to separate out the trap concentration: the spectral density was normalized with the square of the current and multiplied by the active volume. Here, the active volume is assumed to be the undepleted channel thickness, which was obtained from capacitance-voltage measurements. Fig. 4.3 shows that, based on this normalization, the average trap concentration is found to increase with reverse gate bias. This is expected if the trap observed is not uniformly distributed but instead increases in concentration towards the oxide interface. It is noted here that there are large uncertainties in the assignment of numerical values to the density of traps in the MESFET structure because the noise power depends on the square of the current density, which varies significantly within the device structure. Moreover, it was assumed that the main g-r noise mechanism is due to the trapping/de-trapping in the MESFET channel.

However, charge fluctuations in the space charge region causing fluctuations of the conducting channel thickness will lead to equivalent noise spectra. [12] It is therefore hard to distinguish between these mechanisms, but the conclusion that the mid-gap trap is more concentrated close to the interface holds in either cases. In addition, it is still possible to state that the density of the mid-gap trap is higher in the 40-μm than the 100-μm wide devices compared in Fig. 4.3. This is consistent with the above finding that the signal is undetectable in the 300 μm device. These observations qualitatively support the assignment of the trap to an oxidation-induced defect injected from the interface. Further, the results imply that the introduction of the mid-gap state depends on the over-oxidation time rather than the total oxidation time. That means that the trap is introduced efficiently only after the entire layer has been oxidized, providing an important clue regarding its microscopic origin.

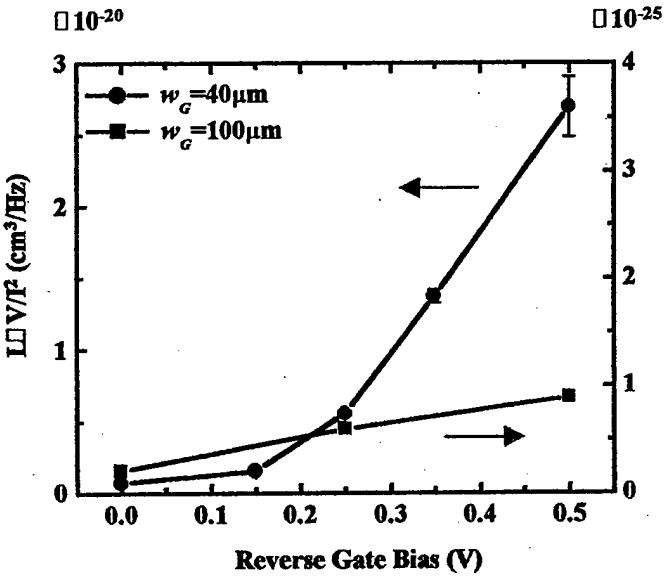


*Figure 4.3: Gate bias dependence of the normalized Lorentzian noise amplitude $L \times V/I^2$ in GOI MESFETs with different gate widths (T=375 K, $V_D$= 0.2 V).*

The observed near mid-gap level is tentatively identified by way of the similar values of the energy level and the cross section as the level EB4 (also referred to as E4); the emission characteristics of this electron trap [1] are shown in Fig. 4.2 by the dashed line and fit the g-r noise data well. The trap was first observed in 1 MeV electron-irradiated GaAs. [13] EB4 has also been observed in non-irradiated GaAs, e.g. in GaAs grown by molecular-beam epitaxy (MBE) at low temperature (380-400°C). [14, 15] EB4 is generally assumed to be due to a complex of the arsenic-antisite ($As_{Ga}$) and another defect that is not an intentional n-type doping impurity. Electron paramagnetic resonance studies of the arsenic-antisite arsenic-vacancy ($As_{Ga}$-$V_{As}$) complex have speculated that EB4 could arise from an electronic transition of $As_{Ga}$-$V_{As}$. [16] This assignment would be in agreement with calculations of the thermal emission rate of such a complex. [17]

During lateral wet-oxidation of AlAs As-rich conditions are realized in the neighboring GaAs, as evidenced by TEM [7] observations of arsenic precipitates in the

vicinity of the oxide interface. A possible cause could be found in the *oxidation of GaAs* after the AlAs is consumed. Defects related to $As_i$, $V_{Ga}$, $As_{Ga}$, and complexes thereof, would be expected to dominate under such conditions. An assignment of the EB4 level to $As_{Ga}$-$V_{As}$, which could possibly result from the conversion $V_{Ga} \leftrightarrow As_{Ga}$-$V_{As}$ predicted by the amphoteric defect model, [18] would provide a possible mechanism for the introduction of EB4 in GOI MESFETs.

In conclusion, low-frequency generation-recombination noise has been studied in GOI MESFETs for different over-oxidation conditions. Three clear defect levels were found, and one ($E_C$-0.69 eV) was identified with a previously reported $As_{Ga}$-related defect (EB4). This defect appeared after the AlAs layer has been fully oxidized. The spatial distribution was shown to increase towards the oxide interface, suggesting that this defect is introduced into the channel as a result of the oxidation process.

This work was supported by the AFOSR, Grant No. F49620-01-1-0151.

### 4.2 Radiation Tolerance of GOI MESFETs

The wide application of wet lateral oxidation of aluminum arsenide buffer layers was mentioned in the previous section. Additionally to its dependence on the oxidation process, the radiation tolerance of this relatively novel technology was investigated.

Devices were obtained through the collaboration with the MURI at the University of California, Santa Barbara. A chief benefit of this technology is the reduced buffer leakage, resulting in record power added efficiencies. In order to explore systematically the radiation tolerance of the $Al_2O_3$ layer and the interface with GaAs, we fabricated GOI MESFETs with different oxidation times as well as standard GaAs reference MESFETs at the UC Berkeley Microfabrication Laboratory.

Device DC parameters including threshold voltage, drain saturation current, and transconductance were studied on all MESFETs before and after 55MeV proton-induced damage. Proton irradiation with fluences ranging from $5.4 \times 10^{12}$ to $6 \times 10^{13}$ $cm^{-2}$ were carried out at Lawrence Berkeley National Lab's 88-Inch Cyclotron.

Finally, low-frequency noise measurements were carried out to obtain the microscopic evidence of both bulk radiation-induced defects and defects in the vicinity of the GOI interface. We plan to correlate low-frequency noise spectroscopy with other characterization techniques, such as deep level transient spectroscopy, time-resolved photo luminescence, and Hall effect, to develop a detailed model of the failure mechanism in GOI MESFETs.

The variation of the drain current $I_d$, transconductance $g_m$, and threshold voltage $V_t$ with proton fluence was investigated on conventional reference MESFETs and GOI MESFETs with different over-oxidation. All the devises showed similar fluence dependence. Drain current and transconductance, both taken at zero gate bias, degrade with proton fluence. Within the given errors, the transconductance reduction with fluence is equal to the drain current reduction. Moreover, the threshold voltage remains almost unchanged upon irradiation, with perhaps a small increase. The fluence dependence seems to indicate that the displacement damage of 55 MeV proton irradiation is dominated by mobility reduction and it is independent of buffer oxidation conditions.

From the DC characteristics, MESFETs using GOI technology have similar radiation hardness as conventional MESFETs and the radiation hardness does not change with different amounts of over-oxidation.

Nevertheless, low-frequency noise measurement shown in Figure 4.4 reveals a fluence dependence that is absent in DC characteristic in the present proton-fluence range. The 1/f noise spectral density is normalized with the square of the current to compare devices with different widths. The fluctuation of the data depends significantly on different fabrication runs even with identical process flow. However, the 1/f noise component clearly shows a higher noise level on GOI MESFETs and more degradation with radiation than conventional MESFETs. Its radiation sensitivity is strongly dependent on amount of over-oxidation.

The mechanism of 1/f noise is not yet clear. Even though a detailed model is indeed needed to completely understand the 1/f noise mechanism, the obvious radiation sensitivity dependence on the amount of over oxidation is already revealed.

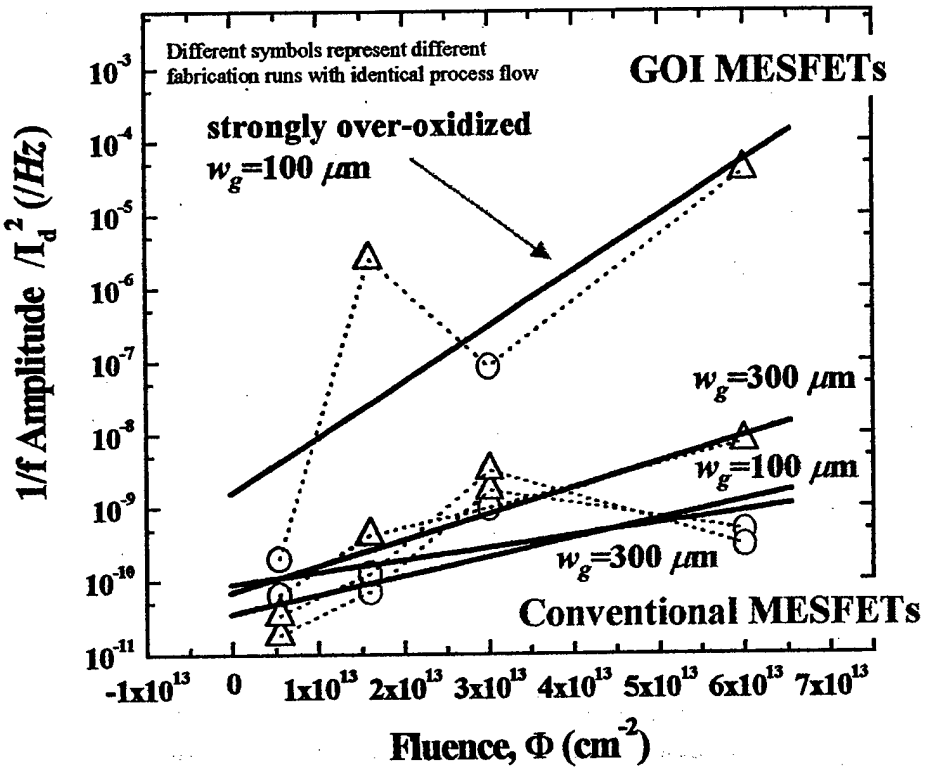


*Figure 4.4: Fluence dependence of 1/f noise component for GaAs-On-Insulator and conventional MESFETs*

From generation-recombination (g-r) noise components, many trap levels could be resolved depending on fluence and over-oxidation. In pre-irradiated samples, three levels were revealed at $E_C$ - 0.7 eV, $E_C$ - 0.47eV, and $E_C$ - 0.32 eV. The mid-gap trap is

identical to EB4, a complex associated with $As_{Ga}$, in both energy level and cross section. The level at 0.47 eV, appearing only at larger gate biases, may be related to surface conduction processes. In 55 MeV proton-irradiated samples, levels at $E_C$-0.79 eV, $E_C$-0.63 eV, and $E_C$-0.54 eV, and $E_C$-0.26 eV were observed. A zoo of defects observed after 55 MeV proton irradiation can be well correlated to the fluence dependence of 1/f noise component, for which one of its physical origin is carrier number fluctuation.

This work was supported by the AFOSR, Grant No. F49620-99-1-0289.

### 4.3 Noise in Carbon-Doped GaN

In MBE grown p-doped GaN epilayers a distinct yellow luminescence signal was found which increased with the carbon doping. Because the yellow luminescence was believed to be always associated with native defects, namely gallium vacancies, $V_{Ga}$, some growth runs were done with varying doping concentrations, accompanied by positron annihilation spectroscopy (PAS) to determine the concentration of $V_{Ga}$. Also, a few tests with carbon-doped GaN, co-doped with silicon, were initiated. Astonishingly, these wafers were n-conductive. The carbon, commonly an acceptor in GaN, could not compensate the silicon donors. The PAS analysis showed that the materials yellow luminescence did not correlate with the concentration of gallium vacancies. The formation of gallium vacancies was largely suppressed with increasing carbon doping. Noise measurements in combination with temperature dependent noise spectroscopy was applied to determine the activation energy of the dominant noise trap in this material.

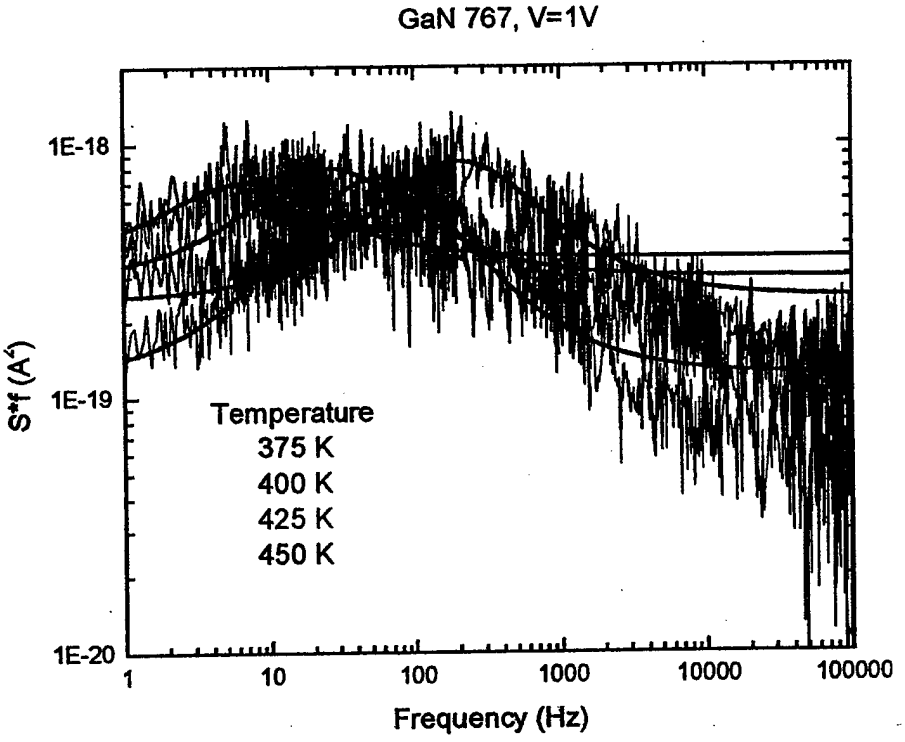


*Figure 4.5: Temperature dependent noise spectroscopy of a GaN MBE grown epilayer doped with carbon and silicon*

The results show a generation-recombination noise which is independent of the applied bias. The temperature dependent spectroscopy in Figure 4.5 gives the signature of a deep level which is located at 0.6 eV below the conduction band (result of the activation energy plotted in Figure 4.6). This defect is only observed in silicon co-doped films and might be correlated with a Si complex. A possible formation of Si-C complexes could explain the failure of the carbon to compensate the silicon donors. However, additional defect characterization is necessary to unambiguously identify this defect.

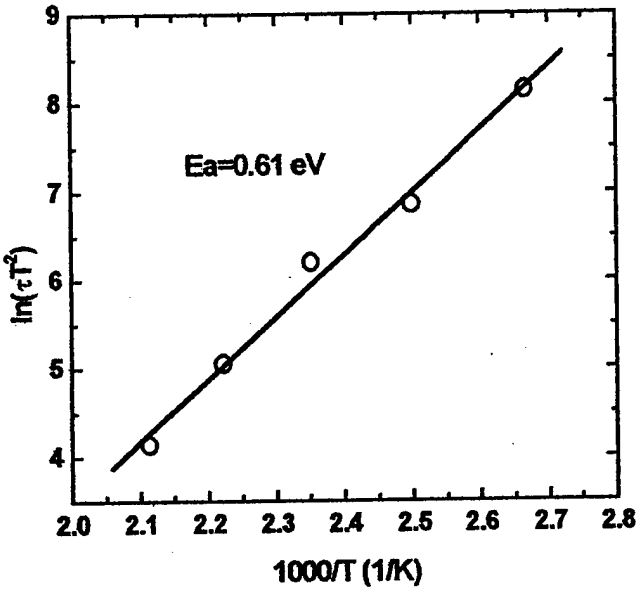


*Figure 4.6: Activation energy of a generation recombination trap obtained from the peak positions of the noise spectra in Figure 4.5*

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# 5. First results – other research groups

## 5.1 Ultra-Thin Body p-MOSFET's with Molybdenum Gate

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Ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFET devices are promising for sub-50 nm CMOS technology. The thin body suppresses short-channel effects and results in performance superior to bulk-Si devices [1]-[3]. To eliminate threshold-voltage variations due to statistical dopant fluctuations, and also to achieve high carrier mobilities for high drive current, it is desirable to use low dopant concentrations in the body. The threshold voltage must then be adjusted by adjusting the gate work function, rather than by channel doping. For fully-depleted SOI technology, the desired range of gate work functions is 4.4 eV to 5.0 eV [4], so that the conventional n+/p+ poly-Si gate technology will not be suitable. Molybdenum (Mo) has recently been shown to be a promising gate material for p-channel MOSFETs [5], [6]. With nitrogen ($N^+$) implantation and subsequent thermal annealing, the work function of a Mo gate electrode can be reduced, so as to become suitable for FDSOI n-channel MOSFETs [7], [8]. Mo is therefore an attractive candidate for single-metal, dual-work-function gate technology, for future CMOS devices. Recently, it has been shown that $N^+$ implantation into Mo-gated MOS diodes can result in damage to the gate oxide, evidenced by increased gate leakage and interface-state density, so that care must be taken to optimize the implant and annealing conditions.

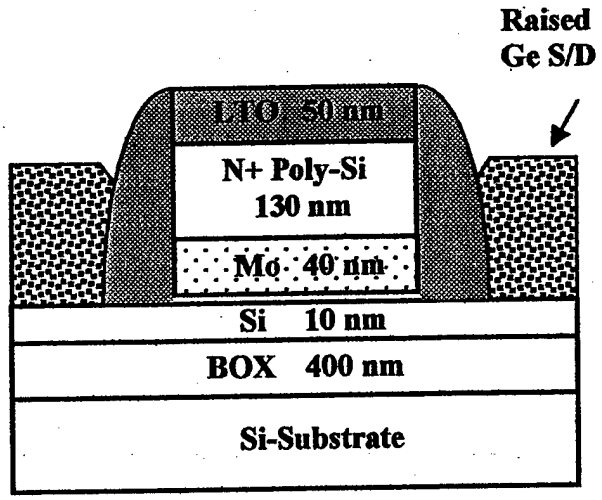



*Figure 5.1: Schematic cross section of the UTB SOI p-MOSFET structure*

The UTB p-MOSFET's used in this work were fabricated on 100 nm-thick p-type ($< 1 \times 10^{15}$ $cm^{-3}$) SOI wafers. The device structure is shown in Fig. 5.1. The buried oxide thickness was 400 nm and the Si film was thinned down to 10 nm by thermal oxidation.

2.5 nm-thick gate oxide was grown at 750 °C and 40 nm-thick Mo gate films were deposited in a DC magnetron sputtering system at 200°C. Some devices then received a nitrogen implant at an energy of 20 keV and a dose of either $2\times10^{15}$ or $4\times10^{15}$ $cm^{-2}$. Then *in-situ*-doped n+ poly-Si and an LTO hard mask layer were deposited. After gate-sidewall spacer formation, Ge was selectively deposited using conventional LPCVD at 350 °C, 300 mTorr [1], and boron was subsequently implanted to dope the source/drain regions. A very conservative RTA at 700 °C for 60 s in $N_2$ ambient was used to activate the implanted dopants, to avoid significant intermixing of Ge and Si [7]. Further details of the device fabrication process have been reported elsewhere [7]. The magnitude of the threshold voltage ($V_{TH}$) was found to increase by ~65 mV for each nitrogen dose increment of $1\times10^{15}$ $cm^{-2}$.

To investigate the $Si/SiO_2$ interface quality of these devices, their low frequency noise characteristics have been measured. Prior to noise analysis, the transistor DC characteristics were measured with a HP4155 semiconductor parameter analyzer. All the measured output drain current noise ($S_I$) were converted to the equivalent gate voltage noise given by the formula $S_{VG} = S_I / (g_m)^2$ where $g_m$ is the measured transconductance.

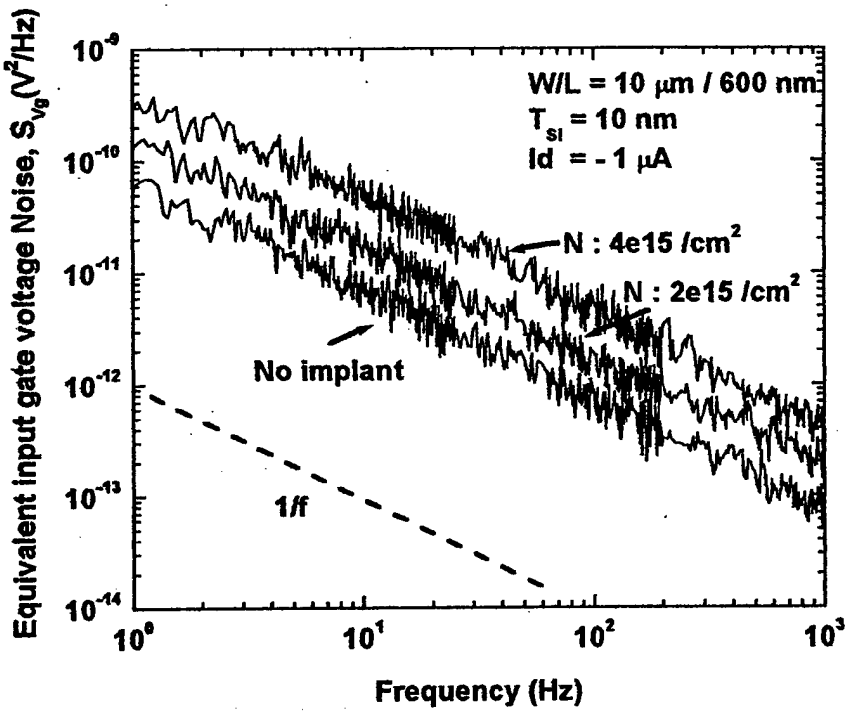
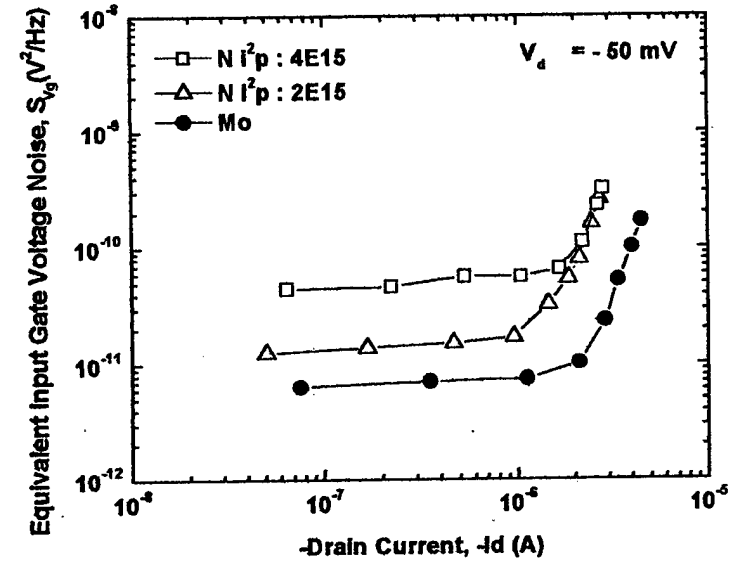


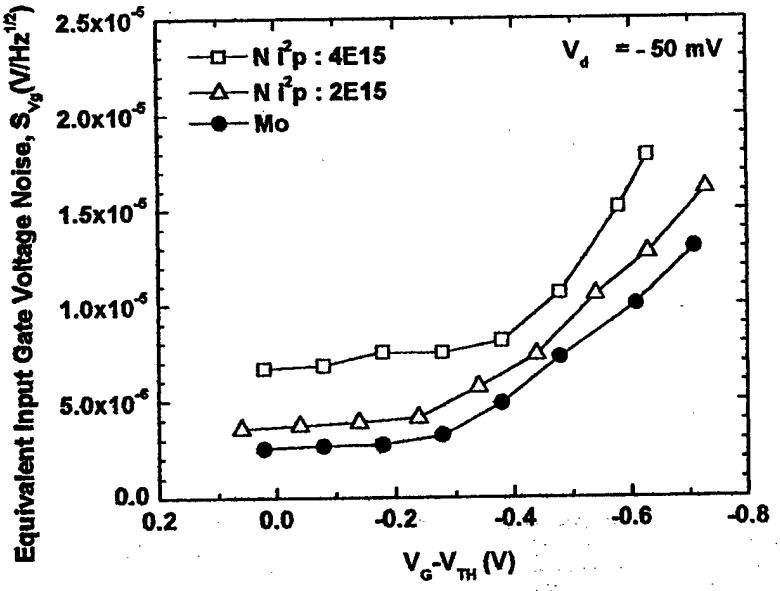

*Figure 5.2: Equivalent input gate voltage noise power spectrum versus frequency for UTB SOI p-MOSFET's biased at Vd = -50mV, Id = -1□A. (W/L = 10 μm / 600 nm).*

Fig. 5.2 shows $S_{VG}$ versus frequency at a drain current level of –1 □A. In all the devices examined, 1/f $^{\gamma}$□ dependence was observed with γ being close to 1, which indicates a uniform spatial distribution of oxide traps near the interface [10]. It is clear from the figure that the noise level increases with the nitrogen implant dose.

Fig. 5.3(a) shows $S_{VG}$ characteristics of the devices measured at 10 Hz as a function of drain current. As can be seen, $S_{VG}$ is almost constant in weak inversion and increases in a quadratic manner in strong inversion. Also, the noise level increases with increasing nitrogen dose, over the entire drain current range. The constant noise behavior in weak inversion suggests that the low frequency noise is mainly due to carrier number fluctuation caused by the traps located near the $Si/SiO_2$ interface. On the other hand, the parabolic increase of $S_{VG}$ in strong inversion is attributed to mobility fluctuation.




(a)




(b)

*Figure 5.3: Equivalent input gate voltage noise characteristics (a) as a function of drain current and (b) as a function of gate voltage at frequency = 10 Hz, Vd = -50mV. (W/L = 10 μm / 600 nm).*

The expression for the carrier number fluctuation model including the correlated mobility fluctuation was recently given by [9]

$$S_{VG} = S_{VFB}\left[1 + \square\,\square_0 C_{OX}\frac{I_d}{g_m}\right]^2 \qquad (5.1)$$

with

$$S_{VFB} = \frac{\lambda kTq^2 N_t}{fWLC_{OX}^2} \qquad (5.2)$$

where $\square$ is the Coulomb scattering coefficient, $\square_0$ the low-field mobility, $C_{OX}$ the gate capacitance, $S_{VFB}$ the flat-band voltage noise density associated with interface charge fluctuation, $\square$ the tunneling attenuation length (~1Å), $kT$ the thermal energy, $f$ the frequency, $WL$ the device area, and $N_t$ the trap density ($eV^{-1}cm^{-3}$). In strong inversion where $V_G$-$V_{TH} > 0$, by replacing $I_d / g_m$ by $C_{OX}(V_G\text{-}V_{TH})$ [9], (5.1) can be rewritten as,

$$S_{VG} = S_{VFB}\left[1 + \square\,\square_0 C_{OX}(V_G\text{-}V_{TH})\right]^2 \qquad (5.3)$$

Fig. 5.3(b) shows $S_{VG}^{1/2}$ versus gate voltage measured at 10Hz. The linear increase of $S_{VG}^{1/2}$ with respect to $V_G - V_{TH}$ clearly supports the validity of the carrier number fluctuation model with correlated mobility fluctuation in UTB SOI p-MOSFET devices. From this figure, one can extract the parameter $\square$ from the slope and $S_{VFB}$ from the intercept on the horizontal axis, respectively. The oxide trap density, $N_t$ is also extracted from $S_{VFB}$ using Eq. (5.2). The value of $\square$ found from the slope is $5 \times 10^4$ Vs/C for all devices, showing no dependence on nitrogen dose. It is noted that this value is similar to that of bulk p-MOS devices [11].

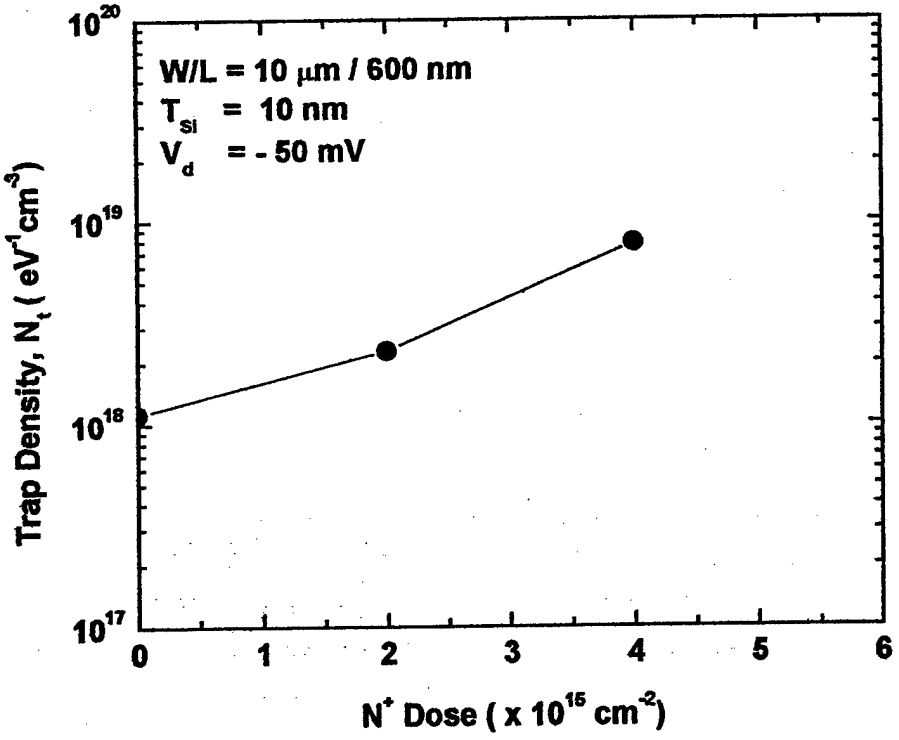


*Figure 5.4: Oxide trap density versus nitrogen gate-implant dose. (W/L = 10 μm / 600 nm).*

Fig. 5.4 shows the oxide trap density, $N_t$ extracted from the flat-band voltage noise data, as a function of N implant dose. The trap density for UTB p-MOSFET's without the nitrogen implant has been found to be $1 \times 10^{18}$ $eV^{-1}cm^{-3}$, which is about one order of magnitude higher than that of conventional poly-Si p-MOS bulk device [11]. It is likely that the traps are mainly caused by sputtering damage during Mo film deposition and can be reduced by using the CVD method [12]. For the nitrogen-implanted devices, the trap density increases exponentially with the nitrogen dose, to $2.3 \times 10^{18}$ and $7.8 \times 10^{18}$ $eV^{-1}cm^{-3}$ for $N^+$ dose of $2 \times 10^{15}$ and $4 \times 10^{15}$ $cm^{-2}$, respectively. This suggests that a considerable amount of nitrogen ions are incorporated in the bulk oxide and at the $Si/SiO_2$ interface during the implantation, due to channeling. By performing the implant at a large tilt angle and lower energy, this effect can be mitigated [8]. Optimization of post-implant thermal annealing should also help to repair damage caused by implantation, and will be necessary before Mo gate technology can be applied in the manufacture of sub-50nm CMOS devices in the future.

Low frequency noise characteristics of Mo-gated UTB SOI p-MOSFET's have been investigated. The observed noise behavior is in excellent agreement with the number fluctuation model with correlated mobility fluctuations. The oxide trap density at the $Si/SiO_2$ interface can be extracted from the noise measurements. The results for a non-optimized Mo gate process indicate relatively high trap density (~one order of magnitude higher than that of conventional poly-Si gated devices), which increases exponentially with $N^+$ gate-implant dose.

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## 5.2 p-channel FinFET's

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Low frequency noise is an important parameter for analog and RF applications. For example, low frequency noise in MOS devices is up-converted to oscillator phase noise, degrading system performance [1]. An increase in the fluctuation of the noise level and deviation from 1/f behavior has been reported as MOSFET dimensions are scaled down [2]. Recently, fully depleted (FD) silicon-on-insulator (SOI) devices have been widely demonstrated and show promise for high-speed [3], analog [4], and RF applications [5]. The FinFET, which has a double-gate straddling a narrow silicon fin, is a candidate structure for FD-SOI technology. High-performance nanoscale FinFET's with excellent short-channel behavior have recently been demonstrated [6], [7].

Standard (100) SOI wafers (p-type, 15 Ω·cm) were used as the starting material. The 100 nm silicon film was thinned to 50 nm, with a 50 nm thermal oxide remaining on top to serve as a hard mask. Fins of extremely narrow and uniform width (beyond the lithographic limit) were obtained with the spacer lithography process [6][7]. Following a sacrificial oxidation of the fin sidewalls, a 2.1 nm gate oxide was grown. Then, either Molybdenum (Mo) (40 nm-thick, deposited by a DC magnetron sputtering at 200 °C and $10^{-7}$ Torr) or $n^+$ poly-Si was deposited as the gate material. After patterning and etching the gate stack, S/D implantation and 900 °C RTA for 60 sec were performed. Further details of this device fabrication process have been reported elsewhere [6]. Fig. 5.5 shows

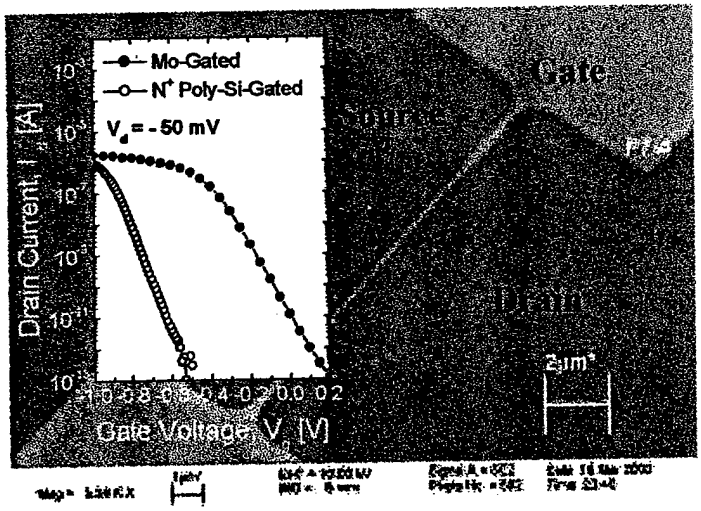


*Figure 5.5: Tilted SEM photographs of double-gate p-FinFET's with Mo-gate ($L_g$ = 400 nm and $W_{fin}$ = 50 nm). Subthreshold $I_d$-$V_g$ characteristics for p-FinFETs with Mo-gate and $n^+$ poly-Si-gate are shown in inset.*

a top-view SEM picture of a p-FinFET comprised of 6 fins, with effective channel width 0.6 □m (= 2 sides × 6 fins × 0. 05 □m fin height). Subthreshold characteristics for p-

FinFETs are shown in the inset. Mo-gated p-FinFET shows lower threshold voltage due to the higher work function of Mo film (~ 5 V) [7].

Prior to noise analysis, the FinFET DC characteristics were measured with a HP4155 semiconductor parameter analyzer. Low frequency noise behavior was then measured over the frequency range of 1 Hz to 10 kHz.

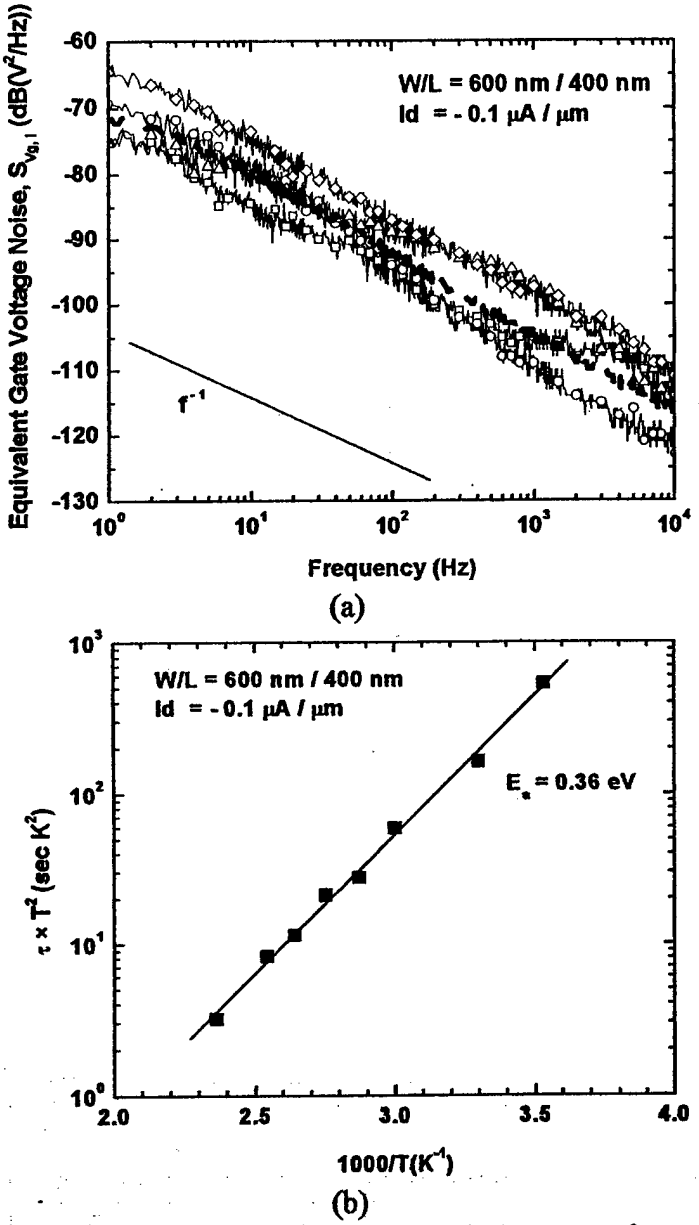


*Figure 5.6: (a) Equivalent gate voltage noise versus frequency in four p-FinFET's with Mo-gate biased at $V_d$ = -50 mV and $I_d$ = -0.1 □A/□m and (b) variation of (□ × $T^2$) versus 1000/T in a p-FinFET with Mo-gate. The dashed line in (a) is the average noise spectra using Equation (1) with N=10.*

Fig. 5.6(a) shows the equivalent gate voltage noise spectra, $S_{VG}$, versus frequency for Mo-gated p-FinFETs with channel area 0.24 □m$^2$. The measured noise spectra from four devices at the drain current level of –0.1 □A/□m are shown. Large deviations in noise level among these devices are observed, which are mainly due to the statistical fluctuation of the number of interface traps confined in the small device area [2]. Such variations in noise spectra are also observed in the measured $S_{VG}$ of poly-Si-gated p-FinFETs. The average equivalent gate voltage noise, $\overline{S_{VG}}$ expressed in dB, is calculated from N = 10 devices by

$$\overline{S_{VG}} = \frac{1}{N}\sum_{i=1}^{N} S_{VG,i} \tag{5.4}$$

where $S_{VG,i}$ denotes the equivalent gate voltage noise of the *i-th* device. The calculated $\overline{S_{VG}}$ is characterized by 1/f $^{\gamma}$ dependence, with $\gamma$ varying between 1 and 1.2 in the frequency range 1 Hz to 10kHz.

For each individual noise curve, one or two generation-recombination (GR) noise humps are seen to be superimposed on the 1/f noise. The GR noise hump is caused by capture and emission of carriers by a single trap, and its characteristics vary with temperature. One GR hump noise was selected and its temperature behavior was examined. Fig. 5.6(b) shows the Arrhenius plot showing the temperature dependence of the GR noise. From this figure, an activation energy ($E_a$) of 0.35 eV and a capture cross section (□) of 2 × 10$^{-21}$ cm$^2$ were extracted from the slope and the intercept of the □ × T$^2$ axis, respectively [8].

The expression for the carrier number fluctuation model including correlated mobility fluctuation was recently given in [9]:

$$S_{VG} = S_{VFB}\,[1 + \square\,\square_0 C_{OX}(V_G - V_{TH})]^2 \tag{5.5}$$

where

$$S_{VFB} = \frac{\lambda kTq^2 N_t}{f^{\gamma} WLC_{OX}^2} \tag{5.6}$$

□ is the Coulomb scattering coefficient, □$_0$ is the low-field mobility, $C_{OX}$ is the areal gate capacitance, $S_{VFB}$ is the flat-band voltage noise density associated with interface charge fluctuation, □ is the tunneling attenuation length (~1 Å), $kT$ is the thermal energy, $f$ is the frequency, □ is the frequency exponent, $WL$ is the device area, and $N_t$ is the trap density (units: eV$^{-1}$cm$^{-3}$). To characterize the statistical fluctuation in noise spectra, the standard deviation □$_{SVG}$ is calculated in dB as

$$\square_{SVG} = \sqrt{\frac{\sum_{i=1}^{N}(S_{VG,i} - \overline{S_{VG}})^2}{N-1}} \tag{5.7}$$

where the $S_{VG}$ values are expressed in dB.

Fig. 5.7 shows the comparison of $\overline{S_{VG}}$ characteristics of the p-FinFETs with n$^+$ poly-Si gates and Mo gates, measured at 10 Hz as a function of gate voltage. The error bars indicate 2□-values. For p-FinFET's with poly-Si gate, $\overline{S_{VG}}$ is almost constant in weak

inversion and increases in a quadratic manner in strong inversion, which clearly supports the validity of the carrier number fluctuation model with correlated mobility fluctuation.

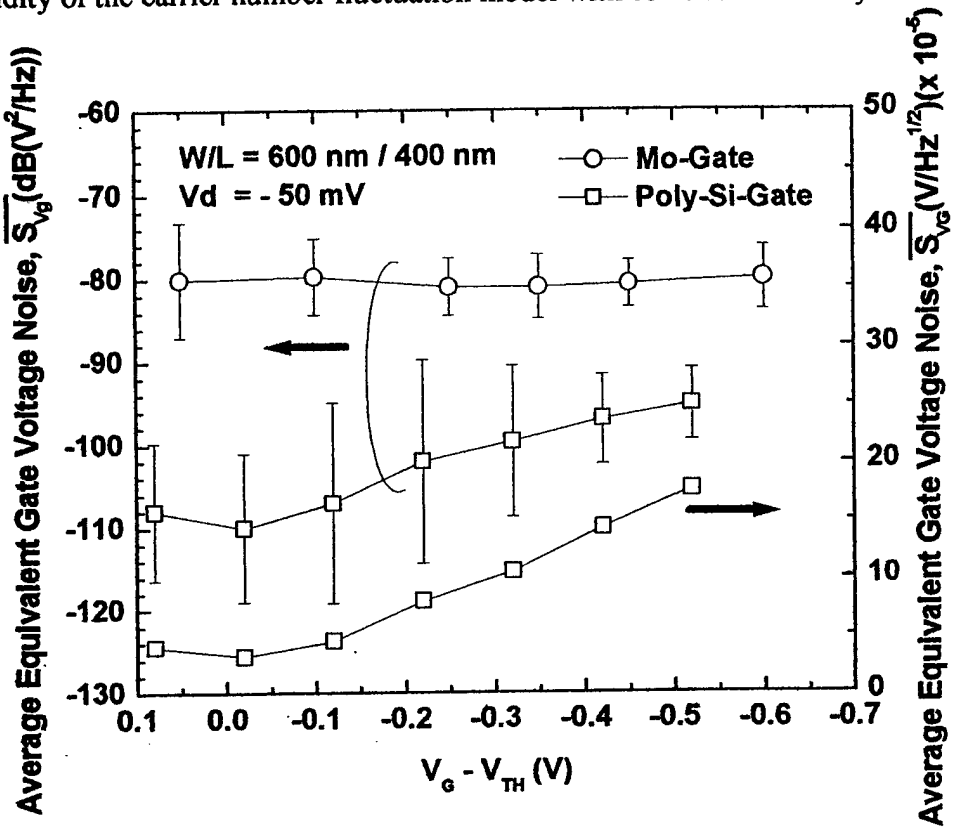


*Figure 5.7: Equivalent gate voltage noise characteristics as a function of gate voltage at $f = 10$ Hz and $V_d = -50$ mV. Symbols and the error bars are calculated from Equation (5.4) and (5.7), respectively.*

On the other hand, for p-FinFET's with Mo gate, $\overline{S_{VG}}$ is almost constant from weak inversion to strong inversion, which suggests that the low frequency noise is mainly dominated by the carrier number fluctuation due to higher interface trap density. From this figure, one can extract the average interface trap density, $\overline{N_t}$ using Eq. (5.5), (5.6), and (5.7) at $(V_G-V_{TH}) = 0$. The extracted trap density of $1.5 \times 10^{17}$ $eV^{-1}cm^{-3}$ for p-FinFET's with poly-Si gate is comparable to bulk-Si MOSFET's [10]. The high average interface trap density of $1 \times 10^{20}$ $eV^{-1}cm^{-3}$ for p-FinFET's with Mo gate is attributed to sputtering damage during Mo film deposition and can be reduced by using the CVD method [11] and adequate thermal annealing. Fig. 5.8 shows $\overline{S_{VG}}$ characteristics of poly-Si-gated p-FinFETs, measured at 10 Hz as a function of drain voltage at $(V_G-V_{TH}) = -0.1$ V. The noise is found to be independent of the drain voltage without excess noise, which suggests that the p-FinFET is fully depleted with no impact ionization [12].

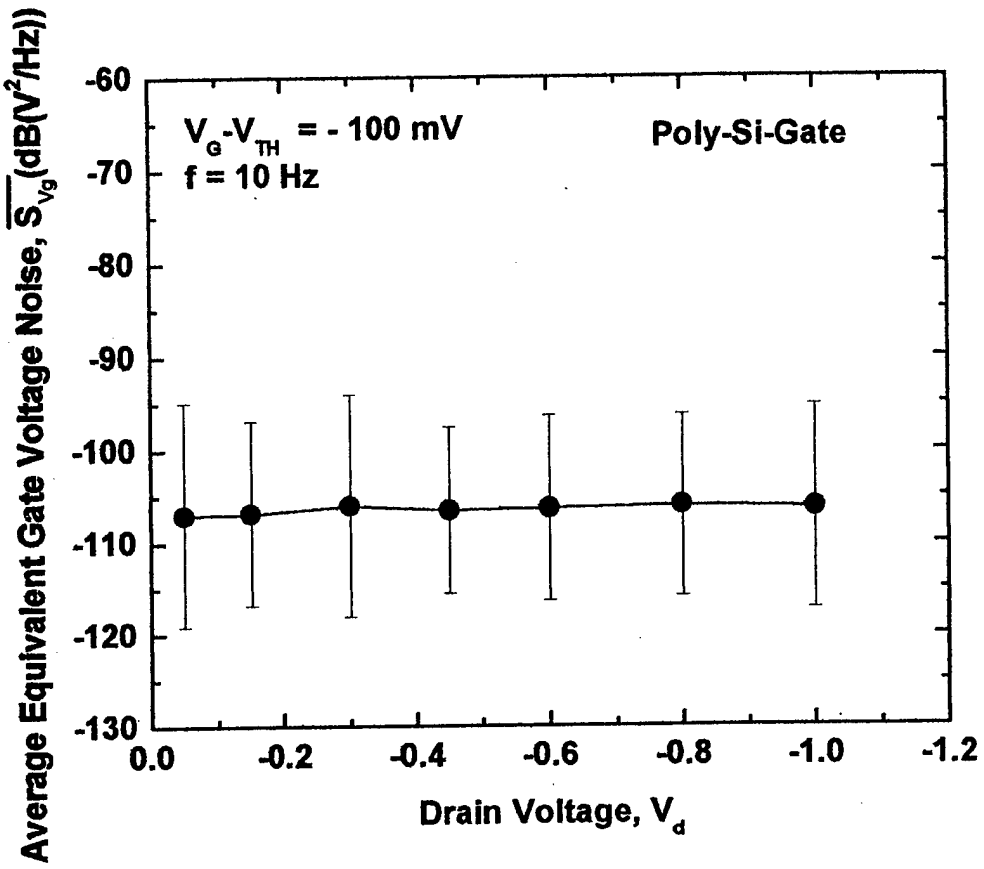


*Figure 5.8: Equivalent gate voltage noise characteristics as a function of drain voltage at f = 10 Hz and $V_G$-$V_{TH}$ = -100 mV. The solid symbol and the error bars are calculated from Equation (1) and (4), respectively.*

Low frequency noise characteristics have been investigated in FinFETs for the first time. Due to the small device area, the measured noise exhibits device-to-device fluctuations by more than one order of magnitude. Although generation-recombination (GR) noise components are observed, the average noise is found to follow a 1/f variation. The low frequency noise behavior in p-FinFET's with poly-Si gate is well described by the carrier number fluctuation with correlated mobility fluctuation.

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# 6. Conclusions

The low-frequency noise measurement system acquired with the DURIP grant was installed and has in the last 18 months successfully applied to several challenging problems in a wide variety of devices and materials. From this work already, and even more considering research planned with this system in the future it can be safely concluded that this new tool has a significant impact on semiconductor research at UC Berkeley, as it allows to combine studies of device performance with the analysis of defects that deteriorate the device performance.

# 7. Future work

## 7.1 Investigations of InP/InGaAs Interface Quality

Due to increasing demand for higher data rates in telecommunication applications, field effect and bipolar transistors need to operate at higher frequencies to achieve performance of above 40 Gbit/s in integrated circuits. InP-based transistors are attractive for several reasons: better substrate thermal conductivity providing a better thermal management, lower surface recombination velocity offering scaling capability, elimination of DX center related traps and the availability of highly-selective wet etchants for convenient fabrication. However, the growth of abrupt InP following InGaAs interface, is a challenge because of the source memory effect. The abruptness of the InP-InGaAs interface impacts directly the performance of the emitter-base junction of heterojunction bipolar transistors and the 2-D electron gas of high electron mobility transistors. The correlation of relevant growth conditions and the low-frequency noise, a key parameter of these transistors when applied in the nonlinear applications where the 1/f noise level is up-converted to phase noise, will be investigated to realize the optimum growth conditions for good interface quality.

## 7.2 Continuing Studies of GaAs-Based MESFETs

Following the low-frequency noise study of GOI MESFETs, a detailed study will focus on the influence of different buffer layers on noise in GaAs MESFETs. Buffer layers to be investigated include semi-insulating GaAs, low-temperature grown GaAs, and reference non-oxidized AlAs layers. The goal of this study is to define a common theme of noise sources related to interfaces.

## 7.3 Electrical Characteristics of Hafnium Oxide Gate Dielectric

As MOSFET device dimensions are scaled down, hafnium oxide is a good alternative to silicon dioxide in effectively reducing the gate leakage current. Hafnium oxide has a high dielectric constant and good thermal stability. One of the challenges is to produce a good $HfO_2$-silicon interface. The traps (charged or neutral) at the interface or in the oxide can degrade the transistor performance by reducing the gain and causing signal delay. The low frequency noise behavior will be studied on transistors with a hafnium oxide

gate dielectric, and used as a tool to investigate the gate dielectric properties with different fabrication processes.

### 7.4 Noise Spectroscopy in III-Nitride Based Devices

Nitride-based electronic devices are attractive for their potential for high output power and high temperature operation. For high performance, low phase noise amplifier applications, the noise behavior is at least as important a figure of merit as the mobility and the charge density of the two-dimensional electron gas (2DEG) in determining the device performance. In AlGaN/GaN HFETs, the 2DEG is formed by spontaneous polarization (depending on the Al concentration) and no doping is required. We will fabricate HFETs with different AlxGa1-xN compositions and thickness to study how polarity effects in AlxGa1-xN/GaN HFETs can impact device performance. The results may be compared with noise figures of devices obtained from industrial partners.

A second field of interest is the radiation tolerance of III-nitride based devices. First studies show a considerable radiation hardness of nitride-based devices [1][2]. However, the epilayer's radiation tolerance is sensitively dependent on the growth process and, therewith, likely on the stoichiometry of the material. Noise spectroscopy of as-grown and irradiated III-nitride devices may give further information on the dominant defects present in the material.